Claims

What is claimed is:

1. A memory cell configured to be coupled to a first control line, at least one second control line and at least one bitline for selectively accessing the memory cell, the memory cell comprising:

a write switch having a control terminal and first and second terminals, the first terminal of the write switch coupled to the at least one bitline, the control terminal of the write switch coupled to the first control line;

a two terminal semiconductor device having first and second input terminals, the first input terminal of the two terminal semiconductor device coupled to the second terminal of the write switch, and the second input terminal of the two terminal semiconductor device coupled to the at least one second control line, wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first input terminal relative to the second input terminal is above a threshold voltage and to have a lower capacitance when the voltage on the first input terminal relative to the second input terminal is less than the threshold voltage;

a read select switch having a control terminal and first and second terminals, the control terminal of the read select switch coupled to the at least one second control line, the first terminal of the read select switch coupled to the at least one bitline; and

a read switch having a control terminal and first and second terminals, the control terminal of the read switch coupled to the first input terminal of the two terminal semiconductor device and coupled to the second terminal of the write switch, the first terminal of the read switch coupled to the second terminal of the read select gate, and the second terminal of the read switch coupled to ground.

2. The memory cell of claim 1, wherein the two terminal semiconductor device comprises a gated diode having a gate input and a source input, the gate input

being the first input terminal of the two terminal semiconductor device and the source input being the second input terminal of the two terminal semiconductor device.

3. The memory cell of claim 2, wherein the gated diode comprises an insulator formed between a gate and a well, a source diffusion region abutting and overlapping one side of the insulator and gate, and a shallow trench isolation region abutting another side of the insulator and gate, wherein the source input of the gated diode is coupled to the source diffusion region and the gate input of the gated diode is coupled to the gate.

4. The memory cell of claim 2, wherein the gated diode comprises an insulator formed between a gate and a well, a first source/drain diffusion region abutting and overlapping one side of the insulator and gate, a second source/drain diffusion region abutting and overlapping another side of the insulator and gate, and an interconnect that electrically couples the first and second source/drain diffusion regions, wherein the source input of the gated diode is coupled to the first source/drain diffusion region and the gate input of the gated diode is coupled to the gate.

5. The memory cell of claim 2, wherein the gated diode comprises an insulator formed between a well and a gate comprising a trench, and comprises a source diffusion region abutting at least a portion of the insulator, wherein the source input of the gated diode is coupled to the source diffusion region and the gate input of the gated diode is coupled to the gate.

6. The memory cell of claim 2, wherein the gated diode is an n-type gated diode.

7. The memory cell of claim 2, wherein the gated diode is a p-type gated diode.

8. The memory cell of claim 1, wherein the two terminal semiconductor device comprises a gated diode having a well and wherein the threshold voltage can be modified by modifying a dopant level in the well of the gated diode.

9. The memory cell of claim 1, wherein the write switch, read select switch, and read switch are Field Effect Transistors (FETs), each FET having a gate and two source/drain diffusion regions, a respective gate coupled to a respective control terminal, and each of respective source/drain diffusion region coupled to one of a respective first or second terminal.

10. The memory cell of claim 9, wherein the write switch, read select switch, read switch, and gated diode are n-type FETs.

11. The memory cell of claim 9, wherein the write switch, read select switch, read switch, and gated diode are p-type FETs.

12. A memory array comprising:

a plurality of first control lines;

a plurality of second control lines;

a plurality of bitlines;

a plurality of ground lines; and

a set of memory cells, each of the memory cells comprising:

a write switch having a control terminal and first and second terminals, the first terminal of the write switch coupled to at least one of the bitlines, the control terminal of the write switch coupled to the one of the first control lines;

a two terminal semiconductor device having first and second input terminals, the first input terminal of the two terminal semiconductor device coupled to the second terminal of the write switch, and the second input terminal of the two terminal

semiconductor device coupled to the at least one second control line, wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first input terminal relative to the second input terminal is above a threshold voltage and to have a lower capacitance when the voltage on the first input terminal relative to the second input terminal is less than the threshold voltage;

a read select switch having a control terminal and first and second terminals, the control terminal of the read select switch coupled to the at least one second control line, the first terminal of the read select switch coupled to at least one of the bitlines; and

a read switch having a control terminal and first and second terminals, the control terminal of the read switch coupled to the first input terminal of the two terminal semiconductor device and coupled to the second terminal of the write switch, the first terminal of the read switch coupled to the second terminal of the read select gate, and the second terminal of the read switch coupled to a ground line.

13. The memory array of claim 12, wherein the plurality of bitlines comprises a plurality of read bitlines and a plurality of write bitlines, wherein a given one of the read bitlines is coupled to the first terminal of the read select switch for a subset of the memory cells and a given one of the write bitlines is coupled to the first terminal of the write switch for the subset of the memory cells.

14. The memory array of claim 12, wherein the plurality of bitlines comprises a plurality of single bitlines, each of the single bitlines coupled to the first terminal of the read select switch for a subset of the memory cells and to the first terminal of the write switch for the subset of the memory cells.

15. The memory array of claim 12, wherein the plurality of second control lines are a plurality of single second control lines, each of the single second control lines coupled to a subset of the memory cells.

16. The memory array of claim 12, wherein the plurality of second control lines comprises a plurality of read select control lines and a plurality of second write control lines, wherein a given read select control line is coupled to the control terminal of the read select switch for a subset of the memory cells, and a given second write control line is coupled to the second terminal of the gated diode for the subset of the memory cells.

17. The memory array of claim 12, wherein the array comprises rows and columns, wherein each subset of two memory cells in two given columns share a given ground line, and wherein there is at least one ground line per two columns.

18. The memory array of claim 12, wherein the array comprises rows and columns, wherein each subset of memory cells in multiple columns share a given ground line, and wherein multiple columns share one of the ground lines.

19. The memory array of claim 12, wherein the two terminal semiconductor device comprises a gated diode having a gate input and a source input, the gate input being the first input terminal of the two terminal semiconductor device and the source input being the second input terminal of the two terminal semiconductor device.

20. The memory array of claim 19, wherein the gated diode comprises an insulator formed between a gate and a well, a source diffusion region abutting and overlapping one side of the insulator and gate, and a shallow trench isolation region abutting another side of the insulator and gate, wherein the source input of the gated diode is coupled to the source diffusion region and the gate input of the gated diode is coupled to the gate.

21. The memory array of claim 19, wherein the gated diode comprises an insulator formed between a gate and a well, a first source/drain diffusion region abutting and overlapping one side of the insulator and gate, a second source/drain diffusion region abutting and overlapping another side of the insulator and gate, and an interconnect that electrically couples the first and second source/drain diffusion regions, wherein the source input of the gated diode is coupled to the first source/drain diffusion region and the gate input of the gated diode is coupled to the gate.

22. The memory array of claim 19, wherein the gated diode comprises an insulator formed between a well and a gate comprising a trench, and comprises a source diffusion region abutting at least a portion of the insulator, wherein the source input of the gated diode is coupled to the source diffusion region and the gate input of the gated diode is coupled to the gate.

23. The memory array of claim 19, wherein the gated diode is an n-type gated diode.

24. The memory array of claim 19, wherein the gated diode is a p-type gated diode.

25. A method for accessing a given memory cell configured to be coupled to a first control line, at least one second control line and at least one bitline, the method comprising the steps of:

modifying a voltage on the at least one second control line from a first voltage to a second voltage, the at least one second control line coupled to the given memory cell of a plurality of memory cells, the given memory cell comprising:

a write switch having a control terminal and first and second terminals, the first terminal of the write switch coupled to the at

least one bitline, the control terminal of the write switch coupled to the first control line;

a two terminal semiconductor device having first and second input terminals, the first input terminal of the two terminal semiconductor device coupled to the second terminal of the write switch, and the second input terminal of the two terminal semiconductor device coupled to the at least one second control line, wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first input terminal relative to the second input terminal is above a threshold voltage and to have a lower capacitance when the voltage on the first input terminal relative to the second input terminal is less than the threshold voltage;

a read select switch having a control terminal and first and second terminals, the control terminal of the read select switch coupled to the at least one second control line, the first terminal of the read select switch coupled to the at least one bitline; and

a read switch having a control terminal and first and second terminals, the control terminal of the read switch coupled to the first input terminal of the two terminal semiconductor device and coupled to the second terminal of the write switch, the first terminal of the read switch coupled to the second terminal of the read select gate, and the second terminal of the read switch coupled to ground; and

returning the voltage on the at least one second control line to the first voltage.

26. The method of claim 25, wherein the method is a method for reading the given memory cell, the method further comprising the step of:

determining a data value corresponding to a state of the at least one bitline.

27. The method of claim 26, wherein:

the method further comprises the step of charging the at least one bitline to a predetermined voltage; and

the step of determining a data value corresponding to a state of the at least one bitline further comprises determining a change in state of the at least one bitline, whereby no change in state is assigned a first data value and a change in state is assigned a second data value.

28. The method of claim 26, wherein:

the at least one control line is a single control line.

29. The method of claim 28, wherein the first voltage is a predetermined low voltage and the second voltage is a predetermined high voltage.

30. The method of claim 25, wherein:

the at least one control line comprises a write control line and a read select control line.

31. The method of claim 30, wherein the step of modifying further comprises the steps of:

modifying the write control line by raising voltage from a predetermined low voltage to a predetermined high voltage; and

modifying the read select control line by raising voltage from a predetermined low voltage to a predetermined high voltage.

32. The method of claim 30, wherein:

the method further comprises the step of placing a signal on the at least one signal line;

the step of modifying further comprises the steps of:

lowering voltage on the write control line from a predetermined high voltage to a predetermined low voltage; and

raising voltage on the write control line from the predetermined low voltage to the predetermined high voltage; and

the method further comprises the step of removing the signal from the at least one signal line, the step of removing the signal performed after the step of lowering voltage.

33. A semiconductor comprising at least one semiconductor memory device, the at least one semiconductor memory device configured to be coupled to a first control line, at least one second control line and at least one bitline for selectively accessing the at least one semiconductor memory device, the at least one semiconductor memory device comprising:

a write transistor comprising an insulator formed between a gate and a well, the gate, and first and second source/drain diffusion regions formed on sides of the gate, the first source/drain diffusion region of the write transistor coupled to at least one bitline, the gate of the write transistor coupled to the first control line;

a two terminal semiconductor device comprising at least a gated diode insulator formed between a gate and a well, the gate, and a source diffusion region that abuts at least a portion of the gated diode insulator, the gate of the two terminal semiconductor device coupled to the second source/drain diffusion region of the write switch, and the source diffusion region of the two terminal semiconductor device coupled to the at least one second control line;

a read select transistor comprising an insulator formed between a gate and a well, the gate, and first and second source/drain diffusion regions formed on sides of the gate, the gate of the of the read select switch coupled to the at least one second control line, the first source/drain diffusion region of the read select transistor coupled to the at least one bitline; and

a read transistor comprising an insulator formed between a gate and a well, the gate, and first and second source/drain diffusion regions formed on sides of the gate, the gate of the read transistor coupled to the first terminal of the gated diode and coupled to the second source/drain diffusion region of the write transistor, the first source/drain diffusion region of the read transistor coupled to the second source/drain diffusion region of the read select gate, and the second source/drain diffusion region of the read transistor coupled to ground.

34. The semiconductor of claim 33, wherein:

the two terminal semiconductor device is a gated diode;

the source diffusion region of the gated diode that abuts at least a portion of the gated diode insulator abuts a first side of the gated diode insulator of the gated diode, the first side of the gated diode insulator being on a first of two sides of the gate of the gated diode; and

the gated diode further comprises a shallow trench isolation region abutting a second side of the gated diode insulator, the second side of the gated diode insulator being on a second of two sides of the gate of the gated diode.

35. The semiconductor of claim 33, wherein:

the two terminal semiconductor device is a gated diode;

the source diffusion region of the gated diode is a first source/drain diffusion region;

the first source/drain diffusion region of the gated diode that abuts at least a portion of the gated diode insulator abuts a first side of the gated diode insulator, the first side of the gated diode insulator being on a first of two sides of the gate of the gated diode; and

the gated diode further comprises a second source/drain diffusion region abutting a second side of the insulator, the second side of the gated diode insulator being on a second of two sides of the gate of the gated diode, and the gated diode further

comprises an interconnect that electrically couples the first and second source/drain diffusion regions.

36. The semiconductor of claim 33, wherein the two terminal semiconductor device is a gated diode, and wherein the gate of the gated diode is formed at least partially in a trench and the insulator separates the trench from the well and the source diffusion region.

37. The semiconductor of claim 36, wherein the trench is cylindrical.

38. The semiconductor of claim 36, wherein the gate of the gated diode further comprises a cap coupled to the trench, wherein the trench underlies the cap and wherein the insulator is formed between portions of the cap not overlying the trench and the well.

39. The semiconductor of claim 36, wherein:

the at least one semiconductor memory device comprises a first semiconductor memory device and the gated diode is a first gated diode having a first source diffusion region;

the semiconductor further comprises a second semiconductor memory device comprising a second gated diode having a second gate at least partially formed in a second trench, a second insulator formed between the second trench and the well, and a second source diffusion region abutting the second insulator; and

the first source diffusion region of the first gated diode is also the second source diffusion region of the second gated diode, whereby the source diffusion area is shared between the first and second semiconductor memory devices.

40. The semiconductor of claim 39, wherein:

the first gated diode has a first trench, first gate, and first insulator;

the first trench underlies a first cap portion of the first gate;

the first insulator is formed between portions of the first cap not overlying the first trench and the well;

the second trench underlies a second cap portion of the second gate; and

the second insulator is formed between portions of the second cap not overlying the second trench and the well.

41. The semiconductor of claim 33, wherein the at least one semiconductor memory device comprises a first semiconductor memory device, the semiconductor further comprises a second semiconductor memory device, and the first source/drain diffusion region of the write transistor is shared between the first and second semiconductor memory devices.

42. The semiconductor of claim 33, wherein the gate of the read select transistor and the gate of the two terminal semiconductor device are contiguous, and wherein the write transistor and the two terminal semiconductor device are separated at least by trench insulation.